

Filtering of Hall B Torus FastDAQ cRIO

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This note presents the changes made to the Torus FastDAQ cRIO to reduce noise in the voltage tap data.

An issue seen in the Hall B Torus voltage tap data is large 60 Hz noise on the signals, despite proper EMC compliance [1]. This is most noticeable on the IDCCT (current transducer) current reading from the magnet power supply when the supply is turned off, Fig. 1.

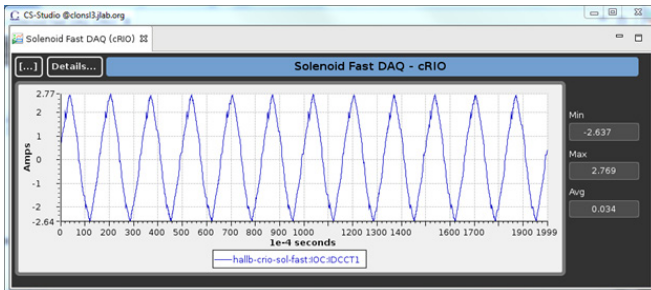


FIG. 1. IDCCT tap with no filtering applied.

Since this effect is seen on all signals to varying degrees, it was decided to add a notch filter on the FPGA with the following parameters: 60 Hz frequency, 20 Q factor, and 10k S/s sample rate, allowing overflow to all the signals. The filter parameters are shown in Fig. 2 and the LabVIEW block diagram is in Fig. 3.

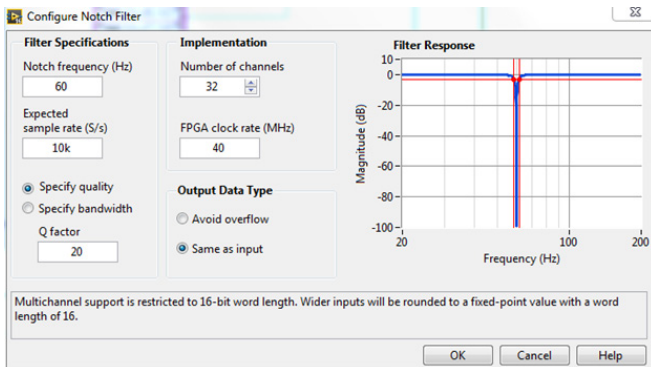


FIG. 2. Notch filter parameters.

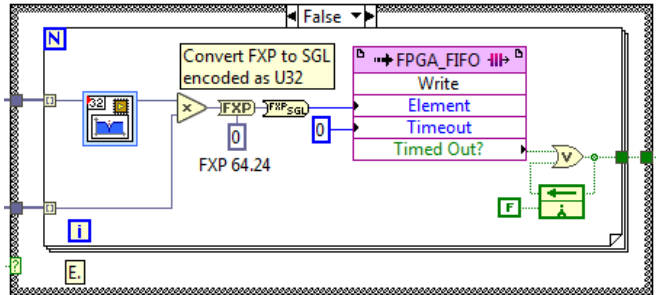


FIG. 3. LabVIEW Block Diagram for FPGA.

Due to the application of the filter on all channels, the bit depth is reduced to 16 bits from 24 bits. Figure 4 shows the resulting tap for IDCCT with the filter applied.

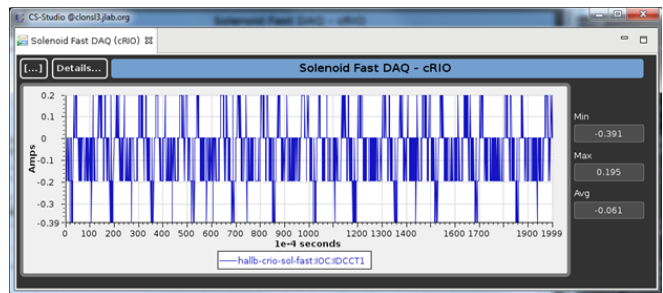


FIG. 4. IDCCT tap with filtering applied..

To conclude, since the majority of the time the voltage tap data is in a steady state, it was decided to leave the filter in place as it results in much less noise in the signals.

[1] <https://logbooks.jlab.org/entry/3452567>.